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EXAMINER	
LIN, WEN TAI	

ART UNIT	PAPER NUMBER
2454	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-INBOX@AKACHANLAW.COM

Office Action Summary	Application No.	Applicant(s)	
	10/708,503	CHEN ET AL.	
	Examiner	Art Unit	
	Wen-Tai Lin	2454	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,45-55 and 59-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,45-49 and 59-67* is/are rejected.

7)☒ Claim(s) *50-55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 45-55 and 59-67 are presented for examination. Claims 56-58 have been canceled in a recent amendment filed 11/10/08.

2. Applicant is recommended to review the language of claim 2, which was amended from an independent claim to depend on claim 1 without deleting the redundancy (e.g., lines 2-3) and revising the antecedence of several associated phrase (e.g., "a method", "a first core", etc.), and make modification to show appropriate antecedent relationship of several phrases between claims 1 and 2.

3. The attempt to incorporate subject matter into this application by merely stating "the references cited in this application" in paragraph 0001 of the specification is ineffective because the reference document is not clearly identified as required by 37 CFR 1.57(b)(2). For example, there are many commercial DSP brand names cited in the specification and in a later stage of the prosecution Applicant indicated that by referencing these commercial DSP chips, their associated data sheets were meant to be included. This is an improper interpretation of the meaning of incorporation-by-reference because the citation of a DSP chip is only a name; it does not represent certain set of documents that Applicant intended to incorporate. In fact there are many different documents, ranging from physical properties to technical implications, that are associated with a DSP chip and data sheet is only one of them.

The incorporation by reference will not be effective until correction is made to comply with 37 CFR 1.57(b), (c), or (d). If the incorporated material is relied upon to meet any outstanding objection, rejection, or other requirement imposed by the Office, the correction must be made within any time period set by the Office for responding to the objection, rejection, or other requirement for the incorporation to be effective. Compliance will not be held in abeyance with respect to responding to the objection, rejection, or other requirement for the incorporation to be effective. In no case may the correction be made later than the close of prosecution as defined in 37 CFR 1.114(b), or abandonment of the application, whichever occurs earlier. Any correction inserting material by amendment that was previously incorporated by reference must be accompanied by a statement that the material being inserted is the material incorporated by reference and the amendment contains no new matter. 37 CFR 1.57(f).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 45-47 and 61-63 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the use of "analog-to-digital converter", "analog input" and "digital-to-analog converter" in claims 45-47 and the use of "phase-locked loop" in claims 61-63 are not described in the specification. This is critical because Applicant's invention is about mapping traffic management tasks into a multi-core DSP integrated-circuit. While it is well known that traffic data are packed as digital data and traffic management deals with the handling of incoming packets (which are in digital format), these added claim limitations are either irrelevant to the claimed subject matter, or the best mode contemplated by the inventor has not been disclosed at the time the application was filed.

Although Applicant argued in recent remarks (filed 11/10/08 and 11/21/08) that the features of "analog-to-digital converter" (A/D), "analog input" and "digital-to-analog converter" (D/A) in claims 45-47 could be found in the data sheets of the commercial DSP chips cited in the specification (for which Applicant claimed that they were properly incorporated by reference), while the "phase-locked loop" (PLL) can be found in Fig. 4. It is noted that even if these added features were incorporated by references (a view point that the examiner respectfully disagrees) and even if the A/D, D/A and PLL are commonly used circuits in DSP chips and some of them may have appeared in some of the drawings (such as Fig. 4, which appears to be a single-core DSP and is therefore irrelevant to Applicant's multi-core DSP as claimed), an ordinary skill in the art would not know how to make and/or use these additional DSP components to achieve the tasks of traffic management because there is no teaching as how these DSP components are related to the implementation/mapping of traffic management on multi-core DSP as claimed.

Claim Rejections – 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

5. Claimed 1-9, 45-55 and 59-67 are rejected under 35 U.S.C. 101 because the claimed invention as a whole does not produce a "useful, concrete and tangible" result to have a practical application. Specifically, the claim languages simply assign traffic management tasks (presumably including the traditional policing, congestion control, scheduling and shaping) on a multi-core DSP integrated circuits without showing further details on how each DSP multi-core is programmed to implement an intended set of algorithms for traffic management. It is important to reveal the details regarding how the DSP architecture is tailored to carry out the intended traffic functions because traditional wisdom indicates that DSP architecture is unfit or ineffective in handling the traffic management tasks. By merely assigning each task to a respective DSP core, it does not solve the effectiveness issue. This is because each DSP resource may be so poorly utilized that it may render the “new approach” useless. If it is meant to make use of parallel processing to improve the execution speed, then the phrase “DSP integrated circuits” may be replaced by any other type of processors and still achieve the same result because multi-core is not an exclusive architectural feature in the DSP world.

Further, it is noted that Applicant’s specification contains only relatively high level mapping of the traffic management tasks [e.g., Figures 7-12], inter-processor communication and event synchronization [e.g., Figures 13-16], and a brief survey as to what DSP chip offers certain instruction to perform a subset of specific task [e.g., Figures 17-21] with different commercial

DSP chips referenced in various embodiments. It raises a doubt as to the possession of the claimed invention at the time of filing because the teaching does not lead to a concrete DSP architecture that an ordinary skill in the art may actually use and make the claimed invention.

Claim Rejections - 35 USC § 103

6. Claims 1-6, 8-9, 45-48 and 59-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (hereafter "Lee") [U.S. PGPub 20030152084] in view of Brown [U.S. PGPub 20040062233] and MSC8101 Data Sheet.

7. As to claims 1-2, Lee teaches the invention substantially as claimed including: a method of managing traffic over a network comprising:

receiving incoming traffic from the network in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory [e.g., paragraphs 19 and 74-75; i.e., each MISD processor has 32 x 64K bytes of instruction memory and 64K registers];

performing a policing function on the incoming traffic to the digital signal processing integrated circuit in a first core of the digital signal processing integrated circuit [e.g., 220a, Fig. 4, paragraph; 76, wherein the first MISD processor (PCU) performs traffic policing];

performing a congestion control function in a second core of the digital signal processing integrated circuit, wherein the second core processes data generated by the first core [e.g., 220b, Fig.4 (i.e., TPU); paragraph 76; note that result of process 222a is fed to its following process 222b]; and

performing a shaping function in a fourth core of the digital signal processing integrated circuit, wherein the fourth core processes data generated by the third core [e.g., 220c (i.e., FPU), Fig.4; paragraph 76].

Lee teaches that the scheduling function in the second core of the digital signal processing integrated circuit together with the congestion control function [paragraph 76]. Lee does not suggest performing the scheduling function in a separate core (i.e., the third core of the digital signal processing integrated circuit).

However, partitioning a task into a plurality of subtasks to be evenly mapped to a plurality of processors for speeding up of execution is well known in the art of parallel processing. It is obvious that Lee's modular MISD arrangement does not have to be limited to only three pipelined stages as shown [see Lee: paragraph 556]. That is, based on Lee's teaching an ordinary skill in the art could have mapped the scheduling and congestion control tasks separately onto different MISD modules if combining these two tasks on a single MISD module becomes a bottleneck. This is because the approach is predictable and the advantage of alleviating processing bottle-neck using additional MISD is obvious. See KSR, 127 S. Ct. at 1742, 82 USPQ2d at 1397.

Further, Lee teaches that the MISD modules together function as a network processor. Lee does not teach that the aforementioned four-stage MISD processors may be replaced by a multi-core DSP integrated circuit.

However, in a similar field of endeavor, Brown teaches that for low channel capacity a single DSP such as MSC8101/MSC8102 (wherein there are four ALUs in the SC-140 core of MSC8101 and there are four SC-140 cores in MSC8102), may implement the task of terminating

packet and circuit switched data streams and other relevant traffic handling, which is traditionally handled by a network processor [e.g., paragraphs 7-14, 19, and 56-70]. Note that in a QoS-enabled cable modem termination system, packet classification, packet prioritization, per-flow policing, congestion control and flow control, fine-grained queuing, scheduling, per-flow traffic shaping etc. are conventionally carried out by a network processor.

Thus, it would have been obvious to one of ordinary skill in the art that at the time the invention was made to have combined the teachings of Lee and Brown by replacing Lee's MISD processors with the four-core DSP chip such as MSC 8102 (as suggested by Brown) because: (1) these Motorola DSP chips are designed with data termination capabilities, with functionalities and inter-processor communication mechanism equipped for packet/data stream processing; and (2) for low channel capacity MSC8101/MSC8102 provide not only the data management but also various DSP functions that are needed in a media engine [see Brown: Fig. 4; see also, e.g., MSC8101 Data Sheet].

8. As to claim 3, Lee further teaches that a traffic management function comprises sorting the traffic by class of service, policing traffic to not exceed boundary of a bandwidth of the channel, and scheduling traffic [e.g., paragraphs 24-25 and 76; Fig. 38] .

9. As to claim 4, Lee further teaches that the scheduling traffic is based on priority queuing, first in first out queuing, class based queuing, round robin, waiting round robin, earlier deadline first, weighted fair queue, deficit round robin, or modified deficit round robin [e.g., paragraphs 261 & 344; note that inherently a queue is order as first-in-first-out].

10. As to claim 5, Lee further teaches that there is no direct communication path between the first core and the second core [e.g., paragraphs 83-84, i.e., the MISD processors are interconnected through buffers or external memory].

11. As to claims 6, 48 and 59-60, Lee further teaches that the data generated by the first core is passed to the second core using a mailbox [e.g., paragraph 84, i.e., "the DBU 292 stores the fixed size buffers into memory and other functional units (such as the FPU) have access to those buffers."].

12. As to claims 61-63, Lee and Brown do not specifically teach the processing involves analog-to-digital (A/D) or digital-to-analog (D/A) conversion. However, since A/D and D/A converters are popular components that many commercial DSP chips have built these types of components on chip. It is obvious that, when so needed, an ordinary skill in the art can easily find an appropriate DSP that is equipped with an D/A, and/or A/D because there are a wide variety of off-shelf DSP chips that are equipped with these components.

13. As to claims 45-47, through Brown's teaching, MSC8101 is equipped with phase lock loop (PLL) circuit [see the MSC8101 Data Sheet]. It is noted, however, PLL is also a popular component that is normally used for keeping the clock of a processor accurate and stable.

14. As to claims 8-9, since the features of these claims can also be found in claims 2, they are rejected for the same reasons set forth in the rejection of claims 2 above.

15. Claims 7, 49 and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al.(hereafter "Lee")[U.S. PGPub 20030152084] and Brown [U.S. PGPub 20040062233], as applied to claims 1-6, 8-9, 48 and 59-60 above, further in view of Bass et al.(hereafter "Bass")[U.S. Pat. No. 6769033].

16. As to claims 7 and 49, Lee teaches that the MISD processor is a data flow machine that is triggered by the availability of data [e.g., paragraphs 73]. Thus, when a plurality of MISD processors are interconnected as shown in Fig. 4, processors (such as 220a – 220c) are synchronized by the arrival of data from a predecessor readying for a next processor [e.g., paragraph 73], wherein each MISD processor uses a timer for stamping the arrival time of incoming data [e.g., Fig. 5; paragraphs 79, 98 and 145].

Lee does not specifically teach using interrupt as triggering mechanism for synchronizing between the first core and second core.

However, in the same field of endeavor, Bass teaches synchronizing the passing of frames among the processors by monitoring input events, Data Buffers available for dispatch, Interrupts and Timers [e.g., col. 9, lines 31-32; col. 21, line 62- col. 22, line 5].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a plurality of timers for triggering Lee's data passing between MISD processors because: (1) interrupt is a well known technique for causing event triggering and synchronization

among different processors, in particular when the processors are associated with different timers; and (2) using interrupt as triggering mechanism facilitates processors synchronization in Lee's data flow model in a sense that the execution of each processor may be triggered by its own local timer (i.e., without relying on a global clock).

17. As to claims 64-67, using Fig. 4 as an example, Lee demonstrates a data flow system where processors (such as 220a – 220c) are synchronized by the arrival of data from a predecessor readying for a next processor [e.g., paragraph 73], wherein each MISD processor uses a timer for stamping the arrival time of incoming data [e.g., Fig. 5; paragraphs 79, 98 and 145]. Bass teaches using interrupt as a triggering mechanism for causing the next processor to execute the available data. Such a triggering mechanism enables the processors to be clocked by their own local timers and uses a predecessor's timer to trigger interrupt for the next processor when data from the predecessor is available.

In light of the teachings of Lee and Bass, it is obvious that an ordinary skill in the art would be able to synchronize a plurality of processors as required in claims 64-67 because no matter how the different processors are mutually interconnected, the triggering mechanism between any processor pair is the same. That is: use a predecessor's timer to trigger interrupt for the next processor when data from the predecessor is available, which has been fully taught by Lee and Bass as described above.

18. Claims 50-55 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 101 and 35 U.S.C. 112, first paragraph, set forth in this Office Action and to include all of the limitations of the base claim and any intervening claims.

19. Applicant's arguments filed on 11/10/08 and 11/21/08 for claims 1-9, 45-49 and 59-67 have been fully considered but they are moot in view of the new grounds of rejection.

Conclusion

Examiner note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the contest of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Tai Lin whose telephone number is (571)272-3969. The examiner can normally be reached on Monday-Friday(8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(571) 273-8300 for official communications; and

(571) 273-3969 for status inquires draft communication.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Tai Lin

January 7, 2009

/Wen-Tai Lin/

Primary Examiner, Art Unit 2454